

United States Patent and Trademark Office



UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,605	12/11/2003	Gary M. Johnson	2008.007900/03-0478 8519	
23720	7590 07/10/2006	EXAMINER		INER .
WILLIAMS, MORGAN & AMERSON			LE, DINH THANH	
	IMOND, SUITE 1100 TX 77042		. ART UNIT	PAPER NUMBER
,			2816	
			DATE MAILED: 07/10/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)			
	10/733,605	JOHNSON, GARY M.			
Office Action Summary	Examiner	Art Unit			
	DINH T. LE	2816			
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply					
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).					
Status	·				
1) Responsive to communication(s) filed on 24 April 2006.					
2a) ☐ This action is FINAL . 2b) ☑ This					
3) Since this application is in condition for allowan					
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.					
Disposition of Claims					
4)⊠ Claim(s) <u>1-10 and 25-44</u> is/are pending in the application.					
4a) Of the above claim(s) is/are withdrawn from consideration.					
5) Claim(s) is/are allowed.					
6)⊠ Claim(s) <u>1-4,9,10,25-28,33-38,43 and 44</u> is/are rejected.					
7) Claim(s) <u>5-8, 29-32 and 39-42</u> is/are objected to.					
8) Claim(s) are subject to restriction and/or election requirement.					
Application Papers					
9) The specification is objected to by the Examiner					
10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.					
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).					
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).					
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.					
Priority under 35 U.S.C. § 119					
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of:					
a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received.					
Certified copies of the priority documents have been received in Application No					
3. Copies of the certified copies of the priority documents have been received in this National Stage					
application from the International Bureau (PCT Rule 17.2(a)).					
* See the attached detailed Office action for a list of the certified copies not received.					
	·				
Attachment(s)					
1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)					
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)					
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5) Notice of Informal Patent Application (PTO-152) 6) Other:					

NON-FINAL REJECTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/24/06 has been entered.

The rejection over the Manning reference (US 5,831,929) is withdrawn in view of the arguments presented in the amendment.

Claim Rejections

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 9-10, 35-38 and 43-44 are rejected under 35 USC 103 (a) as being unpatentable over Lee (US 6,483,359) in view of Johnson et al (US 5,101,17).

Lee discloses in Figures 3-7 a DLL circuit used in a memory device (SRAM, lines 10-23, column 1) comprising:

- a phase detector (320) for comparing an reference clock signal (EXT_CLK) and

Application/Control Number: 10/733605

Art Unit: 2816

Page 3

a feedback signal;

- a coarse delay circuit (340) for switching an activation of a capacitive delay using

switches (345-347, Figure 4);

- a fine delay (360); and

- a feedback delay unit (310).

However, Lee does not disclose that the delay circuit is a transistive capacitive delay.

Johnson et al suggests in Figures 3 and 4 a delay circuit comprising transistive capacitors (72a-

72C) for easily implementing on an integrated circuit to reduce size since the size of the

conventional capacitor is large.

It would have been obvious to a person having skill in the art at the time the invention

was made to employ the transistive capacitor as suggested by Johnson et al in the circuit of Lee

for the purpose of reducing size.

Claims 1-4, 9-10, 25-28, 33-38 and 43-44 are rejected under 35 USC 103 (a) as being

unpatentable over Baker et al (US 6,445,231) in view of Lee (US 6,483,359).

Baker et al discloses in Figures 1 and 14-15 a memory device comprising:

- a first device comprising a memory (102) and a DLL (111); and

a second device (1502) coupled to the first device.

However, Baker does not disclose that the DLL circuit comprising delay circuit as recited

in claim 1.

Nevertheless, Lee in view of Johnson et al suggests in Figure 1 a DLL circuit as stated

above for providing a finer adjustability that would reduce jitter, see lines 5-9, column 1.

Application/Control Number: 10/733605

Art Unit: 2816

Page 4

It would have been obvious to a person having skill in the art at the time the invention

was made to employ the modified DLL circuit of Lee in the circuit of Baker et al for the purpose

of providing a finer adjustability that would reduce jitter.

Response to Applicant's Arguments

The applicant argues that Lee does not disclose that the delay circuit is "transistive

capacitive delay". The argument is persuasive. However, this limitation is suggested in the

Johnson et al reference as stated above.

The applicant argues that there is no motivation to combine the Manning reference with

the Lee reference. The argument is persuasive without traverse.

Allowable Subject Matter

Claims 5-8, 29-32 and 39-42 would be allowable if rewritten to overcome the

rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all

of the limitations of the base claim and any intervening claims.

The claims are allowed because the prior art does not suggest the delay circuit comprising

the inverters and the transistor sets as combined in the claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY CALLAHAN can be reached at (571) 272-1740.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Primary Examiner

6/28/06